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1496.00310

INTEGRATED CIRCUIT WITH ON-CHIP CLOCK FREQUENCY

MATCHING TO UPSTREAM HEAD END EQUIPMENT

Field of the Invention

5   The present invention relates to a satellite or cable transmission system generally and, more particularly, to a method and/or apparatus for implementing an integrated circuit with on-chip clock frequency matching to upstream head end equipment.

Background of the Invention

10   Conventional broadband communication products, such as television set top boxes, have a system clock that is slaved to one or more pieces of upstream head end equipment. Without slaving the clocks, a two clock system would drift. Such drifting could

15   eventually cause an input data buffer and/or an output data buffer within the set top box to overflow or underflow. Additional issues, such as synchronization problems, could also occur.

      Conventional solutions use hardware to compare a timestamp sent from the upstream head end equipment with an on chip

20   local clock timestamp. The difference between the two timestamps

1

is used to generate a difference signal. The difference signal is normally a digital signal that is presented outside of an integrated circuit (IC) seated inside the set top box. The digital difference signal is used to drive a digital to analog (D/A) converter. The digital to analog converter produces an analog signal having a magnitude proportional to the difference of the two timestamps. The analog signal would then drive an external voltage controlled oscillator (VCO). A frequency presented by the VCO is adjusted up or down and used to drive a system clock of the IC of the set top box. A feedback loop is created using external components, such as an analog to digital (A/D) converter, low pass filter and oscillator. Such conventional approaches implement several external discrete components. However, using discrete components creates a high cost and often results in high chip counts.

It would be desirable to match the frequency of a set top box to the frequency of upstream head end equipment by using software within the set top box.

02-0040
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Summary of the Invention

One aspect of the present invention concerns a method for controlling the frequency of oscillation of a local clock signal comprising the steps of (A) generating the clock signal in response to a first control signal, (B) generating the first control signal in response to one of a plurality of adjustment signals selected in response to a second control signal and (C) generating the second control signal in response to a comparison between a local timestamp and an external timestamp.

Another aspect of the present invention concerns an apparatus comprising an oscillator, an adjustment circuit and a tuning circuit. The oscillator may be configured to generate a clock signal in response to a first control signal. The adjustment circuit may be configured to generate the first control signal in response to one of a plurality of adjustment signals selected in response to a second control signal. The tuning circuit may be configured to generate the second control signal in response to a comparison between a local timestamp and an external timestamp.

The objects, features and advantages of the present invention include providing a method and/or apparatus that may (i) implement an integrated circuit having on chip clock frequency

3

matching to upstream head end equipment, (ii) be implemented in software, (ii) be implemented without discrete external components, (iv) be implemented without adding to the cost of a set top box, (v) provide flexibility in set top box design and/or (vi) be implemented in any system needing clock synchronization.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a context diagram illustrating a preferred embodiment of the present invention;

FIG. 2 is a diagram illustrating a controller circuit within a set top box in accordance with the present invention;

FIG. 3 is a more detailed block diagram of the oscillator and tuning section of FIG. 2; and

FIG. 4 is a flow diagram illustrating software in accordance with the present invention.

Detailed Description of the Preferred Embodiments

The present invention may be implemented using software within an on chip embedded controller in a set top box. The present invention may compare the difference between a head end timestamp (e.g., received from a satellite or cable input) and a local timestamp (e.g., generated internally to the set top box). The present invention may be implemented without specific hardware for processing timestamp information.

Referring to FIG. 1, a diagram of a system 100 is shown in accordance with the preferred embodiment of the present invention. The system 100 generally comprises a head end block (or circuit) 102 and a decoder block (or circuit) 104. The decoder block 104 may be implemented as part of a satellite (or cable) set top box. In particular, the decoder 104 may be implemented as a controller implemented within a satellite (or cable) set top box. The head end block 102 generally presents a digital bitstream 110 to a satellite 112. The digital bitstream generally includes an embedded timestamp 114. The satellite 112 may be implemented as a physical satellite orbiting in space. The digital bitstream 110 is generally presented through a transmitter 114 that drives a

transmitting device 116. The transmitting device 116 may be a satellite dish or other appropriate transmitting system.

The circuit 104 may be implemented as a controller circuit (e.g., a chip or integrated circuit) within the satellite set top box. The decoder 104 generally comprises a receiver block (or section) 120 and a processing block (or section) 122. The receiver block 120 may be implemented as a receiver chip connected to an antenna 124. The antenna 124 may be implemented as a satellite receiver antenna or other appropriate receiving device. For example, a typical residential environment uses a variety of satellite antennas such as 18 inch round dishes, 20 inch round dishes, 20 inch elliptical dishes, 22 inch elliptical dishes, etc. Additional satellite antennas are routinely developed (e.g., the multi-LNB "superdish" was recently announced. The present invention is not limited to a particular satellite antenna. The receiver 120 generally receives a signal from one of the low noise blockers (LNB) of the antenna 124. The receiver then presents a digital bitstream 130. In an alternate implementation, the digital bitstream 130 may be received from a cable television system.

In general, the digital bitstream 130 is a replication of the digital bitstream 110. An embedded timestamp 132 may be

present within the digital bitstream 130. The timestamp 132 may be

a replica of the timestamp 114. The decoder 104 may also comprise

a block (or circuit) 140, a block (or circuit) 142, and a block (or

circuit) 144. The block 140 may be implemented to extract a head

5   end timestamp. The block 142 may be implemented to extract a local

timestamp. The block 144 may be implemented as a compare and

adjust chip clock block. The block 140 may generate a timestamp

(e.g., TS1). The timestamp TS1 may be a headend timestamp

representing the timing of the headend block 102. The block 142

10   may generate a timestamp (e.g., TS2). The timestamp TS2 may be a

local timestamp representing the timing of the block 104. The

blocks 140, 142 and 144 may be implemented in software (or

firmware).

The circuit 144 may have an input 150 that generally

15   receives the signal TS1 and an input 152 that generally receives

the signal TS2. The block 104 generally compares the timestamp TS1

with the timestamp TS2. The block 144 generally presents a local

clock signal (e.g., CLK). The circuit 104 may calculate an

adjustment to the timestamp TS1 based on the comparison between the

20   timestamp TS1 and the timestamp TS2. The adjustment may be needed

for the local clock signal CLK to match the timing information from embedded timestamp TS1.

Referring to FIG. 2, a more detailed diagram of the block 144 is shown. The block 144 generally comprises a controller 160, an oscillator 162, a block (or circuit) 164, and a block (or circuit) 166. The block 160 may be implemented as an embedded controller. The block 162 may be implemented as a crystal oscillator. However, other oscillators, such as digital synthesizers with or without a crystal may be implemented to meet the design criteria of a particular implementation. The block 164 may be implemented as a frequency tuning block. The block 166 may be implemented as software control logic. The software control logic block 166 may be used to (i) compare the timestamp TS1 with the timestamp TS2, (ii) calculate a frequency adjustment and (iii) program a number of signals (e.g., CTR) to adjust the frequency of oscillation of the clock signal CLK. The block 166 generally presents the control signals CTR to the block 164, through the controller 166.

The block 164 may be implemented as a multiplexer 180. The multiplexer 180 may have a number of inputs 182a-182n, each configured to receive one of a number of adjustment signals (e.g.,

8

ADJ1-ADJn). The multiplexer 180 generally presents a control signal (e.g., CTR2) by selecting one of the adjustment signals ADJ1-ADJn. The selection is generally controlled by the signal CTR.

5   The block 166 generally receives the signal CLK, the timestamp TS1 and the timestamp TS2 from the controller 160. The block generally presents the signal CTR to the controller 160. The signals CLK, TS1 and TS2 are generally referred to as signals between the controller 160 and the control logic 166. However, the

10   control logic 166 is generally implemented as software (or firmware) that resides on the controller 160. When the block 166 senses the timestamp TS2 is drifting with respect to the timestamp TS1, the block 166 generally calculates the amount of the frequency adjustment to remove the drift. The block 166 presents the control

15   signals CTR to increase or decrease the frequency of the signal CLK.

The comparison of the timestamp TS1 and the timestamp TS2 and adjustment calculation is generally performed within the software block 166. The calculation does not consume very much

20   computing power (e.g., a low MIPs). The software block 166 does

not generally slow down the normal operation of the controller 160.

In general, no additional cost is added to the set top box.

The multiplexer 164 may be digitally controlled. The signals ADJ1-ADJn may each have different effective capacitances.

5 The multiplexer 164 generally enables one of the signals ADJ1-ADJn to be selected to change the frequency of the signal CLK. The particular signal ADJ1-ADJn may be selected in response to the signal CTR. The signal CTR may be a software generated control signal. The embedded controller 160 may be implemented as a

10 microprocessor or microsequencer.

Referring to FIG. 3, a more detailed diagram of the oscillator 162 and the tuning circuit 164 is shown. The tuning circuit 162 is shown as a first portion 162a and a second portion 162b. The oscillator 162 may be implemented as a DCXO (Digitally

15 Controlled Crystal (Xtal) Oscillator). The oscillator 162 may pull up or down a main reference signal (e.g., REF). In one example, the main reference signal REF may be implemented as a 13.5MHz signal. However, other frequencies may be implemented to meet the design criteria of a particular implementation. The 13.5MHz

20 reference signal REF may be used for the all of the Phase Locked Loops (PLLs) in a particular system. The tuning circuit 164a-164b

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may be used to adjust the signal REF. In one example, the tuning

circuit 162a-162b may make adjustments of +150ppm and -150ppm.

However, other adjustments may be used to meet the design criteria

of a particular implementation.

5   The oscillator 160 is similar to a one inverter Pierce

oscillator configuration. A gain stage generally acts as an active

component to sustain the oscillations. For clarity, an inverter

symbol 180 is used in FIG. 3. A feedback resistor 182, a number of

capacitors C1-Cn and the crystal REF generally create a positive

10   feedback, which starts the oscillation. The capacitors C1-Cn are

placed symmetrically around the oscillator 160. The capacitor

banks C1-Cn are generally controlled digitally through a number of

switches (e.g., D1-Dn). Depending on the code in the software 166,

any of the switches D1-Dn may be turned on or off. Once a switch

15   D1-Dn is turned on, the associated capacitor pair is connected to

the both sides of the crystal REF. The oscillation frequency is

inversely proportional to the capacitive load seen by the crystal

REF. If the frequency of oscillation needs to be increased, one or

more of the digital switches D1-Dn are turned off, until the

20   desired frequency range is achieved. To decrease the frequency of

oscillation, one or more of the switches D1-Dn have to be turned

11

on. Since the switches D1-Dn can be controlled easily from the software 166 through the controller 160 the turning off and on process may be software controllable.

Referring to FIG. 4, a flow diagram of a method (or process) 300 is shown in accordance with a preferred embodiment of the present invention. The process generally comprises a state 302, a state 304, a decision state 306, a state 308, a state 310, a state 312, a decision state 314, a state 316, a decision state 318, a state 320 and a state 322.

The state 302 may provide a timeout period to check for a frequency drift. The state 304 generally checks for drifting between the timestamp TS2 and the timestamp TS1. If the difference between the timestamp TS1 and the timestamp TS2 is within a predefined margin, the method 300 moves to the state 322. If the difference between the timestamp TS1 and TS2 is not within the predefined margin, the method moves to state 308. The predefined margin may be target specification for the system 100. For example, a particular system may use a ± 10 ppm (part per million) margin. However, other margins may be implemented to meet the design criteria of a particular implementation. The state 308 generally calculates a frequency adjustment needed to be within the

predefined margin. The state 310 generally calculates a fine tune setting. The fine tune setting may be a value of the control signal CTR that reduces the difference (or drift) between the timestamp TS1 and the timestamp TS2. The state 312 generally sets

5 the fine tuning of the circuit 164. The decision state 314 generally confirms the local timestamp adjustment. If a confirmation is not needed, the method 300 moves to the state 322. If a confirmation is needed, the method 300 moves to the state 316. The state 316 reads and compares to local timestamp TS2 to an

10 expected adjustment. The state 318 checks if there is an error. If there is an error, the state 320 generally posts a message. If there is not an error, the method 300 moves to the state 322. The state 322 generally sets a timeout to check frequency drift.

The function performed by the flow diagram of FIG. 4 may

15 be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present

20 disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention may also be implemented by the preparation of ASICs, FPGAs, or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in

5   the art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can

10   include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

While the invention has been particularly shown and

15   described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.